

IN THE CLAIMS:

The following listing of claims will replace all prior listings of claims in the application:

1. (Currently Amended): A dedicated, hardware-based physics processing unit ~~Physics Processing Unit (PPU)~~ that is coupled to an external memory, comprising:

an internal memory;

a floating point engine (FPE) that includes a vector processor adapted to perform multiple, parallel floating point operations to generate physics data, wherein the multiple, parallel floating point operations are specified by a very long instruction word (VLIW) that is issued issues to the FPE vector processor; [[and]]

a PPU control engine (PCE) configured to control the overall operation of the PPU by allocating memory resources within the internal memory to the FPE and distributing commands received from a host central processing unit (CPU) to the FPE for processing;

a data movement engine (DME) configured to control the movement of data between the external memory and the internal memory in response to instructions received from the PCE; and

a data communication circuit adapted to communicate the physics data to [[a]] the host CPU. Central Processing Unit (CPU).

2. – 3. (Cancelled)

4. (Currently Amended): The PPU of claim 1 ~~[[3]]~~, ~~further comprising: wherein the FPE performs the a Floating Point Engine (FPE) performing~~ multiple, parallel floating point operations on data stored in the internal memory.

5. (Original): The PPU of claim 4, wherein the internal memory is operatively connected to the DME, and further comprising:

a high-speed memory bus operatively connecting an external high-speed memory to at least one of the DME and the FPE.

6. (Original): The PPU of claim 5, wherein the internal memory comprises multiple banks allowing multiple data threading operations.
7. (Original): The PPU of claim 3, wherein the PCE comprises control and communication software stored in a RISC core.
8. (Original): The PPU of claim 5, wherein the internal memory comprises first and second banks, and wherein the DME further comprises:
 - a first unidirectional crossbar connected to the first bank;
 - a second unidirectional crossbar connected to the second bank; and,
 - a bi-directional crossbar connecting first and second crossbars to the external high-speed memory.
9. (Currently Amended): A system, comprising:
 - a central processing unit ~~Central Processing Unit~~ (CPU);
 - an external memory storing data;
 - a dedicated, hardware-based physics processing unit ~~Physics Processing Unit~~ (PPU) coupled connected to the CPU and the external memory and comprising:
 - an internal memory,
 - an application specific integrated circuit ~~Application Specific Integrated Circuit~~ (ASIC) implementing a vector processor adapted to perform multiple, floating point operations, wherein the multiple, parallel floating point operations are specified by a very long instruction word (VLIW) that is issues to the vector processor,[[:]]
 - a PPU control engine (PCE) configured to control the overall operation of the PPU by allocating memory resources and distributing commands received from a host central processing unit (CPU) to the FPE, and
 - a data movement engine (DME) configured to control the movement of data between the external memory and the internal memory in response to instructions received from the PCE, and

~~an external memory storing data, wherein the external memory is communicatively coupled to the PPU.~~

10. (Currently Amended): The system of claim 9, further comprising a personal computer ~~Personal Computer~~ (PC); and wherein the PPU comprises an expansion board adapted for incorporation within the PC, the expansion board mounting the ASIC and the external memory.

11. (Previously Presented): The system of claim 10, further comprising circuitry enabling at least one data communications protocol between the PPU and CPU.

12. (Previously Presented): The system of claim 11, wherein the at least one data communications protocol comprises at least one protocol selected from a group of protocols defined by USB, USB2, Firewire, PCI, PCI-X, PCI-Express, and Ethernet.

13. – 15. (Cancelled)

16. (Currently Amended): The system of claim 9 [[15]], wherein the internal memory is operatively connected to the DME, and further comprising:

a high-speed memory bus operatively connecting the external memory to at least one of the DME and the FPE.

17. (Previously Presented): The system of claim 16, wherein the internal memory comprises multiple banks allowing multiple data threading operations.

18. (Previously Presented): The system of claim 17, wherein the internal memory further comprises:

an Inter-Engine memory transferring data between the DME and FPE.

19. (Previously Presented): The system of claim 18, wherein the internal memory further comprises:

a Scratch Pad memory.

20. (Previously Presented): The system of claim 14, further comprising a command packet queue transferring command packets from the PCE to the DME.

21. (Currently Amended): The system of claim 15, wherein the FPE comprises a plurality of vector floating-point units ~~Vector Floating-point Units~~.

22. (Previously Presented): The system of claim 21, wherein at least one of the command packets defines a vector length of variable length.

23. (Currently Amended): The system of claim 15, wherein the DME comprises a plurality of memory control units ~~Memory-Control Units~~ (MCUs) and a switch fabric ~~Switch Fabric~~ connecting the MCUs to the external memory; and,

wherein the FPE comprises a plurality of vector processing engines ~~Vector Processing Engines~~ (VPEs) receiving data from at least one of the MCUs via a VPE bus.

24. (Currently Amended): The system of claim 23, wherein each VPE ~~Vector Processing Engine~~ (VPE) comprises a plurality of vector processing units ~~Vector Processing Units~~ (VPUs) receiving data from the VPE bus.

25. (Currently Amended): The system of claim 24, wherein each VPU comprises: a dual bank inter-engine memory ~~Inter-Engine Memory~~ (IEM) receiving data from the VPE bus;

one or more data registers receiving data from the IEM under the control of an associated load/store unit ~~Load/Store Unit~~; and

an execution unit ~~Execution Unit~~ performing parallel floating point operations.

26. (Previously Presented): The system of claim 23, wherein at least one command packet received from the PCE defines a vector length of variable length.

27. (Currently Amended): The system of claim 23, wherein the switch fabric ~~Switch Fabric~~ comprises at least one crossbar circuit.

28. (Previously Presented): The system of claim 24, wherein each VPU is dynamically re-configurable.